

Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in this application.

Listing of Claims

1-57. (Cancelled)

58. (New) An electrical circuit for driving an amplifier operative to amplify a differential voltage between a pair of signal lines to a full digital logic separation, said circuit comprising:

a switch coupled between a voltage source and an input terminal of said amplifier, said switch operative to raise said input terminal to a voltage greater than ground potential prior to development of said differential voltage between said pair of signal lines.

59. (New) The electrical circuit of claim 58 wherein said electrical circuit is included in a memory circuit.

60. (New) The electrical circuit of claim 58 wherein said electrical circuit is included in a dynamic random access memory (DRAM) circuit.

61. (New) The electrical circuit of claim 58 wherein said input terminal is a first input terminal of a PMOS transistor, said PMOS transistor having a second input terminal coupled to one of said pair of signal lines and a third input terminal coupled to the other of said pair of signal lines.

62. (New) The electrical circuit of claim 61 wherein said PMOS transistor comprises a low threshold voltage ( $V_{tp}$ ) PMOS transistor.

63. (New) The electrical circuit of claim 62 wherein said  $V_{tp}$  is slightly greater than said differential voltage.

64. (New) The electrical circuit of claim 62 wherein said differential voltage between said pair of signal lines causes said low  $V_{tp}$  PMOS transistor to turn sub-threshold ON.

65. (New) The electrical circuit of claim 58 further comprising at least one transistor operative to maintain said input terminal of said amplifier at about

ground potential prior to said switch raising said input terminal to said voltage greater than ground potential.

66. (New) The electrical circuit of claim 58 further comprising circuitry operative to raise said input terminal of said amplifier to a full supply voltage after said differential voltage develops between said pair of signal lines.

67. (New) The electrical circuit of claim 66 wherein said voltage greater than ground potential is about one-half of said full supply voltage.

68. (New) The electrical circuit of claim 66 wherein said circuitry raising said input terminal of said amplifier to said full supply voltage causes said amplifier to amplify said differential voltage between said pair of signal lines to said full digital logic separation.

69. (New) A method of driving an amplifier operative to amplify a differential voltage between a pair of signal lines to a full digital logic separation, said method comprising:

raising a voltage at an input terminal of said amplifier to a voltage greater than ground potential prior to development of said differential voltage between said pair of signal lines.

70. (New) The method of claim 69 wherein said raising said voltage at said input terminal of said amplifier comprises raising a voltage at an input terminal of an amplifier included in a memory circuit.

71. (New) The method of claim 69 wherein said raising said voltage at said input terminal of said amplifier comprises raising a voltage at an input terminal of an amplifier included in a dynamic random access memory (DRAM) circuit.

72. (New) The method of claim 69 wherein said raising said voltage at said input terminal comprises raising a voltage at a first input terminal of a PMOS transistor, said PMOS transistor having a second input terminal coupled to one of said pair of signal lines and a third input terminal coupled to the other of said pair of signal lines.

73. (New) The method of claim 72 wherein said raising the voltage at an input terminal of said PMOS transistor comprises raising the voltage at an input terminal of a low threshold voltage ( $V_{tp}$ ) PMOS transistor.

74. (New) The method of claim 73 wherein said raising said voltage at said first input terminal of a low threshold voltage ( $V_{tp}$ ) PMOS transistor comprises raising a voltage at a first input terminal of a low threshold voltage ( $V_{tp}$ ) PMOS transistor having  $V_{tp}$  slightly greater than said differential voltage.

75. (New) The method of claim 73 wherein said differential voltage between said pair of signal lines causes said low  $V_{tp}$  PMOS transistor to turn "sub-threshold ON."

76. (New) The method of claim 69 further comprising maintaining said voltage at said input terminal of said amplifier at about ground potential prior to said raising said voltage at said input terminal to said voltage greater than ground potential.

77. (New) The method of claim 69 further comprising raising said voltage at said input terminal of said amplifier to a full supply voltage after said differential voltage develops between said pair of signal lines.

78. (New) The method of claim 77 wherein said raising said voltage at said input terminal of said amplifier to a full supply voltage comprises raising said voltage at said input terminal to a supply voltage about twice said voltage greater than ground potential.

79. (New) The method of claim 77 wherein said raising said voltage at said input terminal of said amplifier to said full supply voltage causes said amplifier to amplify said differential voltage between said signal lines to said full digital logic separation.

80. (New) An electrical circuit for driving an amplifier operative to amplify a differential voltage between a pair of signal lines to a full digital logic separation, said circuit comprising:

means for raising a voltage at an input terminal of said amplifier to a voltage greater than ground

potential prior to development of said differential voltage between said pair of signal lines.

81. (New) The electrical circuit of claim 80 further comprising means for maintaining said voltage at said input terminal of said amplifier at about ground potential prior to said raising said voltage at said input terminal to said voltage greater than ground potential.

82. (New) The electrical circuit of claim 80 further comprising means for raising said voltage at said input terminal of said amplifier to a full supply voltage after said differential voltage develops between said pair of signal lines.